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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/652,044	08/31/2000	Toshimitsu Taniguchi	10417-039001	2951

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EXAMINER
GEBREMARIAM, SAMUEL A

ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 12/02/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application N	Applicant(s)
	09/652,044	TANIGUCHI ET AL.
	Examiner	Art Unit
	Samuel A Gebremariam	2811

-- The MAILING DATE of this communicati n appears on the cover sheet with the correspondenc address --

P riod f r Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 September 2002* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *6-28* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *6-28* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Pri rity under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Objections

1. Claim 7 is objected to because of the following informalities: On line 3 of claim 7 there is a word missing describing the concentration type between "forming" and "concentration". Appropriate correction is required.

2. The claims are objected to because the lines are crowded too closely together, making reading and entry of amendments difficult. Substitute claims with lines one and one-half or double spaced on good quality paper are required. See 37 CFR 1.52(b).

Also use the standard font size as suggested by MPEP.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claim 6, is rejected under 35 U.S.C. 102(b) as being anticipated by Kubo, US patent No. 5,567,629.

Regarding claim 6, Kubo teaches a method of manufacturing a semiconductor device comprising: forming a high concentration source/drain layers (4) and (5) respectively of the reverse conductive type formed in a semiconductor layer (1b) of one conductive type, forming a gate electrode (3) formed on a channel layer located between the source and drain layers (figs. 2A and 2B), and forming a body layer (1C) of one conductive type adjacent to the source layer and a low concentration drain layer of

the reverse conductive type formed between the channel layer and the drain layer, wherein the body layer is formed only under the gate electrode, and wherein forming a body layer of one conductive type comprises a step of doping impurities of one conductive type into the semiconductor layer by ion implantation (figs. 2A and 2B, col. 4, lines 25-67).

Regarding claims 7, 8 and 16, Kubo teaches the entire claimed process of claim 6 above including the above process comprising the steps of doping impurities of the reverse conductive type into the semiconductor layer to forma low concentration drain layer (col. 4, line 63-67) of the reverse conductive type; doping impurities of the reverse conductive type into the semiconductor layer to form a high concentration source layer (4) of the reverse conductive type so that the source layer is adjacent to one end of the gate electrode (3) and form a high concentration drain layer (5) of the reverse conductive type in a position apart from the other end of the gate electrode; doping impurities of one conductive type into the semiconductor layer to form a body layer (1C) of one conductive type extended from under one end of the gate electrode and formed so that the body layer is adjacent to the source layer (4) of the reverse conductive type; and forming a gate electrode (3) on a gate oxide film (2) after the gate oxide film is formed on the semiconductor layer (figs. 2A and 2B, col. 4, lines 25-67).

Claims 22 -26, are rejected under 35 U.S.C. 102(b) as being anticipated by Kubo et al., US patent No. 5,567,629.

Regarding claim 22, Kubo teaches (figs. 2A and 2B) a method of manufacturing a semiconductor device comprising: forming a source/drain regions (4) and (5) of a

second conductive type in a semiconductor of a first conductive type (1B); doping impurities of the first conductive type by ion implantation to form a semiconductor layer (1C) of first conductive type comprising a channel located between the source/drain regions doping impurities of the second conductive type into the surface of the semiconductor layer of the first conductive type to form a second conductive type layer.

Regarding claim 23, Kubo teaches (figs. 2A and 2B) a method of manufacturing a semiconductor device comprising: forming a low concentration source/drain regions of a second conductive type in a semiconductor of a first conductive type (1b), forming a high concentration source/drain regions (4) and (5) of the second conductive type in the low concentration source/drain regions: doping impurities of the first conductive type into the semiconductor of the first conductive type by ion implantation to form the semiconductor layer of the first conductive type (1C) comprising a channel located between the source/drain regions; and doping impurities of the second conductive type into the surface of the semiconductor layer of the first conductive type to form a second conductive type layer.

Regarding claim 24, Kubo teaches (figs. 2A and 2B) the entire claimed process of claim 23 above including the low concentration source/drain regions surround the high concentration source/drain regions and forming a gate electrode (3) on a gate oxide film (2) provided on the semiconductor of the first conductive type wherein the low concentration source/drain regions extends from under the gate electrode.

Regarding claims 25 and 26, Kubo teaches (figs. 2A and 2B) the entire claimed process of claim 24 above including the low concentration source/drain regions of the

second conductive type are formed to be adjacent to the semiconductor layer of the first conductive type formed below the gate electrode by ion implantation.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claim 9, is rejected under 35 U.S.C. 103(a) as being unpatentable over Kubo in view of Chen et al. US patent No. 5,926,712.

Regarding claim 9, Kubo teaches substantially the entire claimed process of claim 7 above except explicitly stating that the low concentration drain layer of the reverse conductive type or the low concentration source/drain layers of the reverse conductive type are formed so that they are shallow under the gate electrode and they are deep under the high concentration drain layer of the reverse conductive type or the high concentration source/drain layers of the reverse conductive type.

It is conventional and also taught by Chen forming a low concentration drain layer (216) that is shallow under the gate and deeper under the high concentration drain region as claimed.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the low concentration drain layer taught by Chen in the method of Kubo.

Claims 10, 11 and 17, are rejected under 35 U.S.C. 103(a) as being unpatentable over Kubo in view of Kao et al. US patent No. 5,688,700.

Kubo teaches substantially the entire claimed process of claims 6 and 7 above including forming a gate electrode (3) on a gate oxide (2) so that the gate electrode covers the body layer (1C).

Kubo does not teach doping impurities of one conductive type into the layer of the reverse conductive type to form a body layer of one conductive type.

It is conventional and also taught by Kao to form a body layer (32) by doping impurities of one conductive type as claimed using ion implantation.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the body layer taught by Kao in the method of Kubo in order to improve breakdown voltage.

Regarding claim 11, Kubo teaches substantially the entire claimed process of claim 10 above including doping an impurity for forming a reverse conductive type layer by ion implantation after forming the body layer (Kao, figs. 15 and 16).

Claims 12-15, 18 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kubo in view of Kao and in further view of Shida US patent No. 6,033,944.

Regarding claims 12 and 13 Kubo teaches substantially the entire claimed process of claim 10 above except explicitly stating forming more than one MOS transistor.

Kubo teaches forming an n-channel MOSFET. It is within one of ordinary skill in the art to realize that it only takes reversing the polarity of the dopants to form p-channel MOSFET.

Furthermore it is conventional and also taught by Shida to form more than one transistor as claimed.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to form more than one MOS transistor in order to make a functional device.

Regarding claims 14,15, 18 and 19, Kubo teaches substantially the entire claimed process of claims 10 and 12 above including using a resist film in an area except areas where the source and drain layers of the MOS transistors are formed as a mask (col. 4, lines 63-67, col. 5, lines 1-12).

Regarding claim 20 and 21, Kubo teaches substantially the entire claimed process of claims 12 and 14 above including the first MOS transistor is a micro MOS transistor; and the second MOS transistor is a MOS transistor having high resistance to voltage.

The limitation that the above transistor is a micro MOS is conventional device that is commonly fabricated in semiconductor fabrication.

With regards to the limitation that the MOS transistor have a high resistance to voltage, this characteristic is considered to be inherent characteristic of most transistors since any layer have a resistance to voltage value.

Claims 27 and 28, are rejected under 35 U.S.C. 103(a) as being unpatentable over Kubo in view of Shida.

Regarding claims 27 and 28, Kubo teaches substantially the entire claimed process of claims 12 and 22-26 above including doping impurities using a resist film, as a mask, to form first and second MOS transistors.

Kubo teaches forming an n-channel MOSFET. It is within one of ordinary skill in the art to realize that it only takes reversing the polarity of the dopants to form p-channel MOSFET.

Furthermore it is conventional and also taught by Shida to form more than one transistor as claimed.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to form more than one MOS transistor in order to make a functional device.

The limitation the semiconductor device comprising a first transistor having high resistance to voltage and a second transistor having high resistance to voltage is not taught Kubo explicitly.

The claimed characteristic is considered to be inherent characteristic of most transistors since any layer have a resistance to voltage value.

Response to Arguments

5. Applicant's arguments with respect to claims 6-28 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

6. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Samuel Admassu Gebremariam whose telephone number is 703 305 1913. The examiner can normally be reached on 8:00am-4: 30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on (703) 305-7646. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 308-7722 for regular communications and (703) 308-7724 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

Samuel Admassu Gebremariam
November 27, 2002

TOM THOMAS
SUPERVISORY PATENT EXAMINER
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